

LH5332600

High-speed 32M-bit Mask-Programmable ROM

Description

The LH5332600N/T (User's No. : LHMN56XX/LHMN5FXX) is a CMOS 32M-bit mask-programmable ROM organized as 4 194 304 × 8 bits (Byte mode) or 2 097 152 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin.

Features

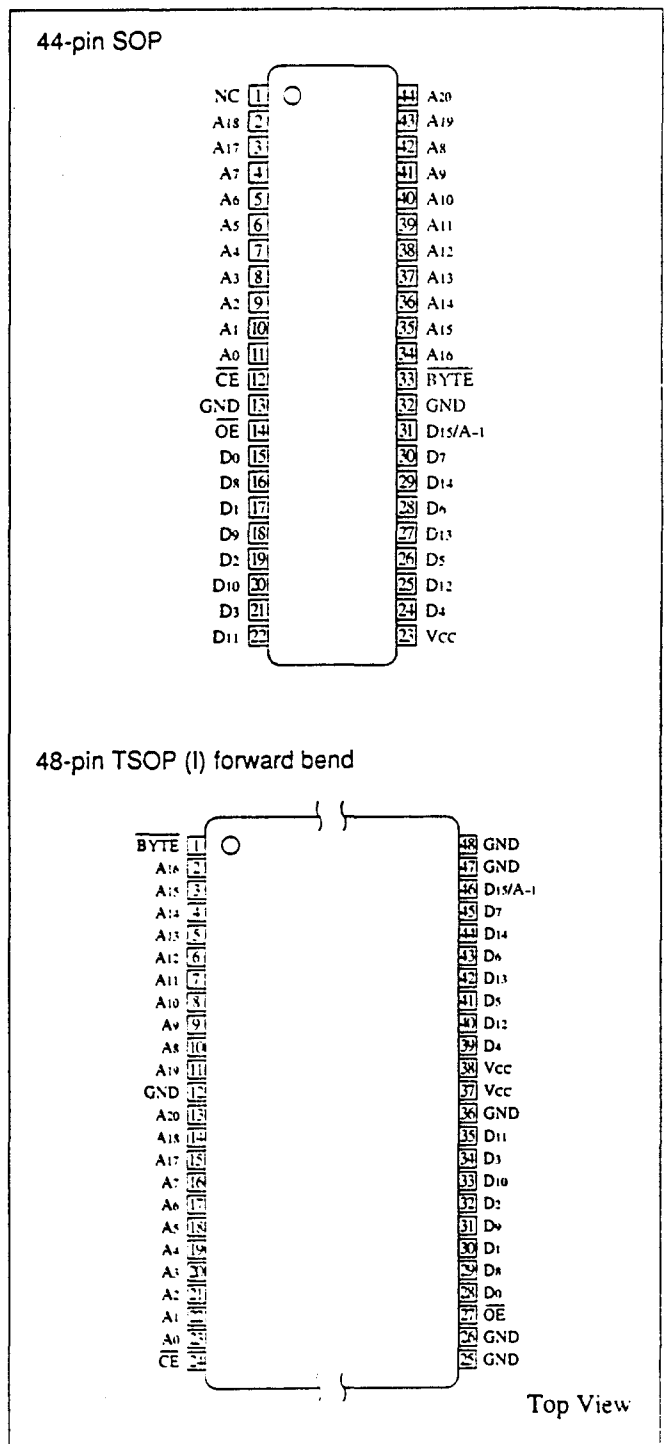
- 4 194 304 × 8 bit organization
(Byte mode : $\overline{\text{BYTE}} = V_{IL}$)
2 097 152 × 16 bit organization
(Word mode : $\overline{\text{BYTE}} = V_{IH}$)
- Maximum access time 100 ns
- Maximum supply current
Operating 100 mA
Standing 100 μ A
- Static operation
- TTL compatible I/O
- Three-state outputs
- Supply voltage 5 V ± 10%
- Package :
LH5332600N 44-pin SOP (SOP044-P-0600)
LH5332600T 48-pin TSOP (I) forward bend (TSOP048-P-1218)

Pin Description

Signal	Pin name	Note
A-1-A20	Address input	1
D0-D15	Data output	
$\overline{\text{BYTE}}$	Byte / word mode switch	
$\overline{\text{CE}}$	Chip enable input	
$\overline{\text{OE}}$	Output enable input	
Vcc	Power supply	
GND	Ground	
NC	No connection	

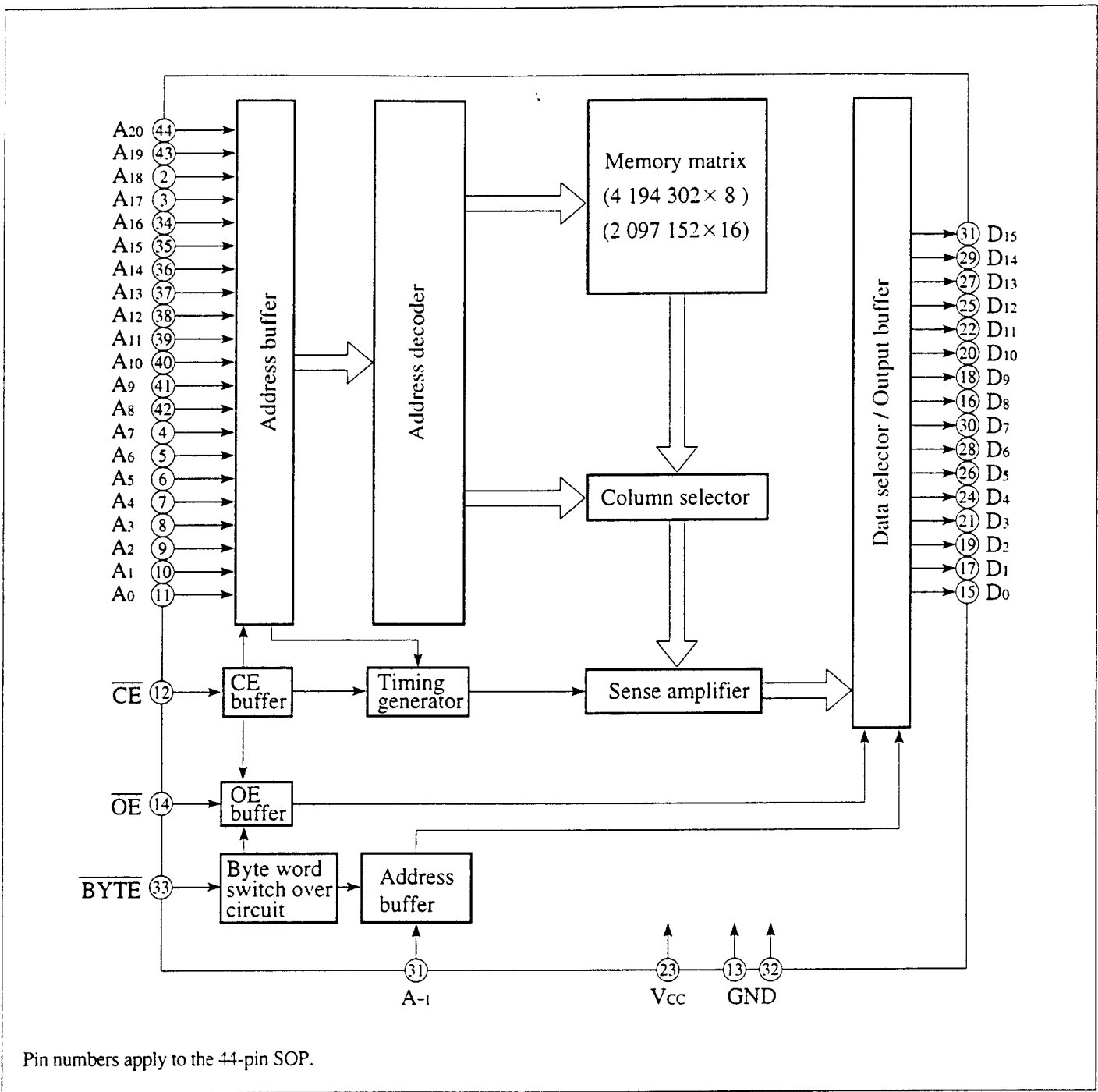
Note 1. D15/A-1 pin becomes LSB address input (A-1) when the bit configuration is set in byte mode, and data output (D15) when in mode. $\overline{\text{BYTE}}$ input pin selects bit configuration.

Pin Connections



LH5332600

■ Block Diagram



■ Truth Table

\overline{CE}	\overline{OE}	\overline{BYTE}	A ₋₁ (D ₁₅)	Data output		Address input		Supply current
				D ₀ -D ₇	D ₈ -D ₁₅	LSB	MSB	
High	X	X	X	High-impedance	High-impedance	—	—	Standby
Low	High	X	X	High-impedance	High-impedance	—	—	Operating
Low	Low	High	Inhibit	D ₀ -D ₇	D ₈ -D ₁₅	A ₀	A ₂₀	Operating
Low	Low	Low	Low	D ₀ -D ₇	High-impedance	A ₋₁	A ₂₀	Operating
Low	Low	Low	High	D ₈ -D ₁₅	High-impedance	A ₋₁	A ₂₀	Operating

X : Don't Care

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to +150	°C

■ Recommended Operating Conditions

(T_a=0 to 70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH}		2.2		$V_{CC} + 0.3$	V	
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Output "High" voltage	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4			V	
Output "Low" voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$			0.4	V	
Input leakage current	$ I_{L1} $	$V_{IN} = 0\text{ V to }V_{CC}$			10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$			10	μA	2
Supply current (Operating)	I_{CC1}	$t_{RC} = 100\text{ ns}$			100	mA	3
	I_{CC2}	$t_{RC} = 1.0\ \mu\text{s}$			90		
Supply current (Standby)	I_{SB1}	$\overline{CE} = V_{IH}$			2	mA	
	I_{SB2}	$\overline{CE} = V_{CC} - 0.2\text{ V}$			100		
Input capacitance	C_{IN}	$f = 1.0\text{ MHz, }T_a = 25\text{ }^\circ\text{C}$			10	pF	
Output capacitance	C_{OUT}				10		

Note 2. $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$

Note 3. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$ Output is open)

AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{RC}	100			ns	
Address time	t_{AA}			100		
Chip enable access timer	t_{ACE}			100		
Output enable delay time	t_{OE}			50		
Output hold time	t_{OH}	5				
Output floating time	t_{CHZ}			40		4
	t_{OHZ}			40		

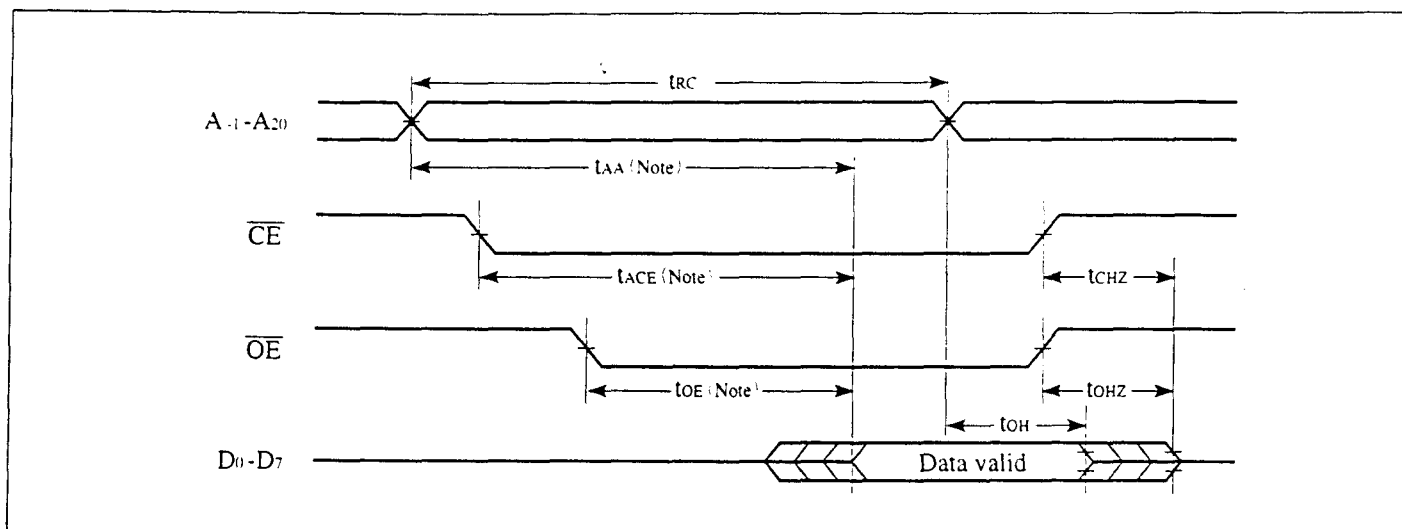
Note 4. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC Test Conditions

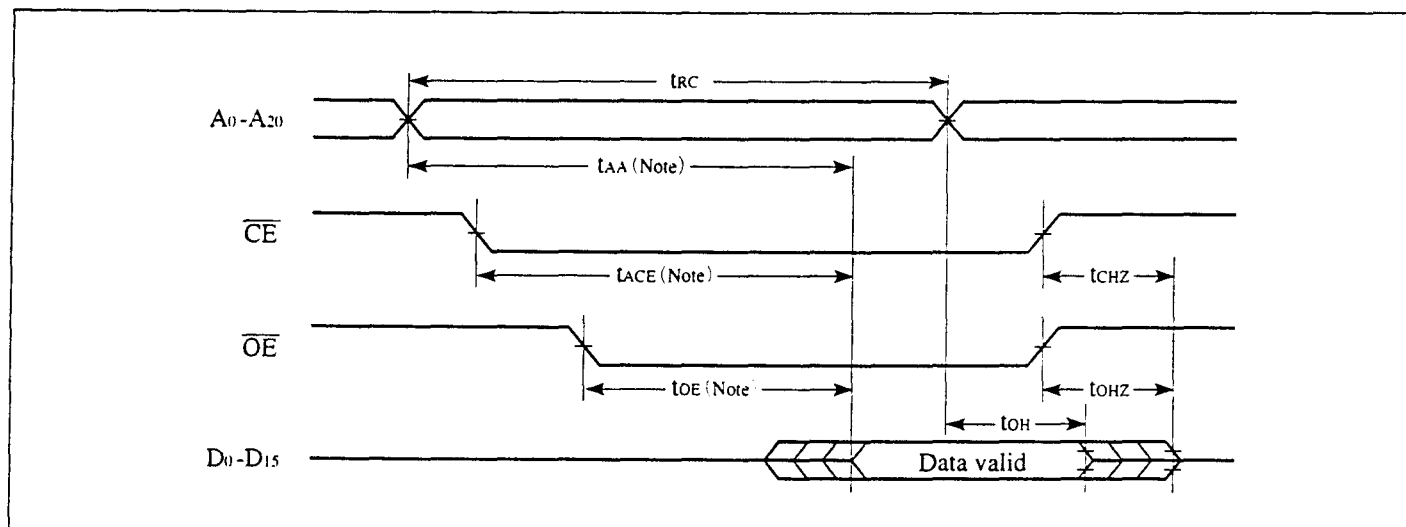
- Input voltage amplitude : 0.4 to 2.6 V
- Input signal rise / fall time : 10 ns
- Input reference level : 1.5 V
- Output reference level : 1.5 V
- Output load condition : 1TTL - 100 pF

■ Timing Diagram

i) Byte mode ($\overline{\text{BYTE}} = \text{VIL}$)



ii) Word mode ($\overline{\text{BYTE}} = \text{VIH}$)



Note. The output data becomes valid when the last interval t_{AA} , t_{ACE} or t_{OE} have concluded.

Sharp's Product Line-up (32M-bit Mask ROM)

★ Under development

Configuration (words × bit)	Pinout*	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MIN.	Supply current (mA) MAX.	Supply voltage (V)	Package
2M × 16	M	LH5332C00D	LHMN5CXX	120	80	5 ± 10%	42DIP
2M × 16	M	LH5332A00AD	LHMN5AXX	150	65	5 ± 10%	42DIP
4M × 8 2M × 16	M	LH5332600N	LHMN56XX	100	100	5 ± 10%	44SOP
4M × 8 2M × 16	M	LH5332600T	LHMN5FXX	100	100	5 ± 10%	48TSOP(I) forward bend
4M × 8 2M × 16	M	LH5332P00N	LHMN5PXX	120	80	5 ± 10%	44SOP
4M × 8 2M × 16	M	LH5332P00T/TR	LHMN5DXX	120	80	5 ± 10%	48TSOP(I) forward bend/ 48TSOP(I) reverse bend
4M × 8 2M × 16	M	LH5332500AN	LH535FXX	150	65	5 ± 10%	44SOP
4M × 8 2M × 16	M	LH53V32500N	LHMV55XX	150	35	2.7 to 3.6	44SOP
4M × 8 2M × 16	M	LH53V32500T/TR	LHMV5BXX	150	35	2.7 to 3.6	48TSOP(I) forward bend/ 48TSOP(I) reverse bend

* M : Mask ROM specific pinout

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